

High-Current Complementary Silicon Power Transistors

... designed for use in high-power amplifier and switching circuit applications.

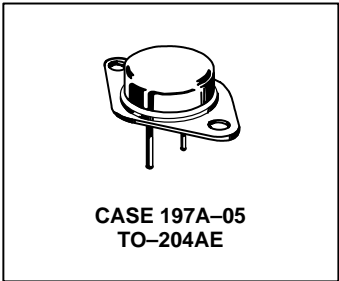
- High Current Capability –
 I_C Continuous = 50 Amperes.
- DC Current Gain –
 $h_{FE} = 15-60 @ I_C = 25 \text{ A dc}$
- Low Collector-Emmitter Saturation Voltage –
 $V_{CE(sat)} = 1.0 \text{ V dc (Max) @ } I_C = 25 \text{ A dc}$

**PNP
2N5684
NPN
2N5686**

**50 AMPERE
COMPLEMENTARY
SILICON
POWER TRANSISTORS
60-80 VOLTS
300 WATTS**

MAXIMUM RATINGS (1)

Rating	Symbol	2N5684 2N5686	Unit
Collector-Emmitter Voltage	V_{CEO}	80	Vdc
Collector-Base Voltage	V_{CB}	80	Vdc
Emmitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current – Continuous	I_C	50	A dc
Base Current	I_B	15	A dc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	300 1.715	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	$^\circ\text{C}$



THERMAL CHARACTERISTICS (1)

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.584	$^\circ\text{C/W}$

(1) Indicates JEDEC Registered Data.

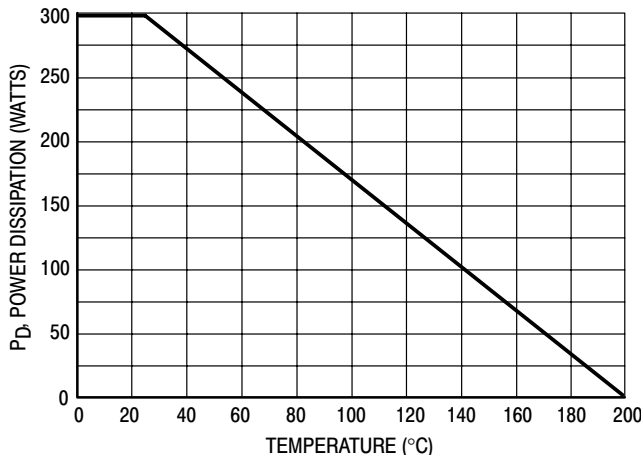


Figure 1. Power Derating

Safe Area Curves are indicated by Figure 5. All limits are applicable and must be observed.

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*ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

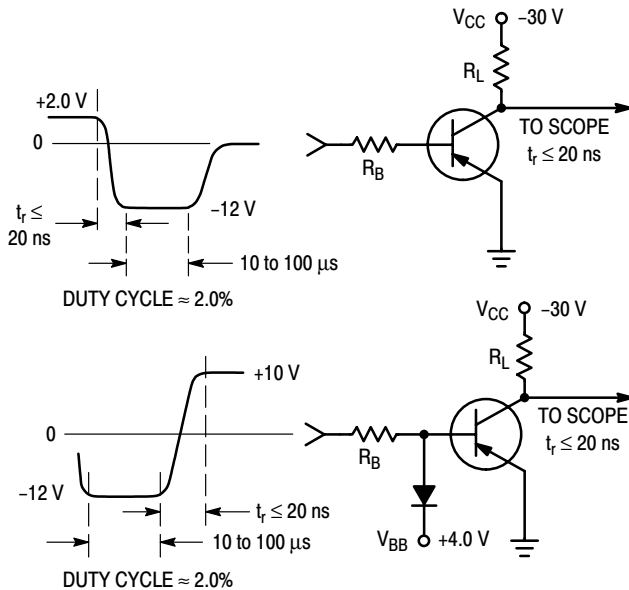
Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (Note 2) ($I_C = 0.2 \text{ Adc}$, $I_B = 0$)	$V_{CEO(sus)}$	80	–	Vdc
Collector Cutoff Current ($V_{CE} = 40 \text{ Vdc}$, $I_B = 0$)	I_{CEO}	–	1.0	mAdc
Collector Cutoff Current ($V_{CE} = 80 \text{ Vdc}$, $V_{EB(off)} = 1.5 \text{ Vdc}$) ($V_{CE} = 80 \text{ Vdc}$, $V_{EB(off)} = 1.5 \text{ Vdc}$, $T_C = 150^\circ\text{C}$)	I_{CEX}	–	2.0 10	mAdc
Collector Cutoff Current ($V_{CB} = 80 \text{ Vdc}$, $I_E = 0$)	I_{CBO}	–	2.0	mAdc
Emitter Cutoff Current ($V_{BE} = 5.0 \text{ Vdc}$, $I_C = 0$)	I_{EBO}	–	5.0	mAdc

ON CHARACTERISTICS				
DC Current Gain (Note 2) ($I_C = 25 \text{ Adc}$, $V_{CE} = 2.0 \text{ Vdc}$) ($I_C = 50 \text{ Adc}$, $V_{CE} = 5.0 \text{ Vdc}$)	h_{FE}	15 5.0	60 –	–
Collector–Emitter Saturation Voltage (Note 2) ($I_C = 25 \text{ Adc}$, $I_B = 2.5 \text{ Adc}$) ($I_C = 50 \text{ Adc}$, $I_B = 10 \text{ Adc}$)	$V_{CE(sat)}$	– –	1.0 5.0	Vdc
Base–Emitter Saturation Voltage (Note 1) ($I_C = 25 \text{ Adc}$, $I_B = 2.5 \text{ Adc}$)	$V_{BE(sat)}$	–	2.0	Vdc
Base–Emitter On Voltage (Note 1) ($I_C = 25 \text{ Adc}$, $V_{CE} = 2.0 \text{ Vdc}$)	$V_{BE(on)}$	–	2.0	Vdc

DYNAMIC CHARACTERISTICS				
Current–Gain – Bandwidth Product ($I_C = 5.0 \text{ Adc}$, $V_{CE} = 10 \text{ Vdc}$, $f = 1.0 \text{ MHz}$)	f_T	2.0	–	MHz
Output Capacitance ($V_{CB} = 10 \text{ Vdc}$, $I_E = 0$, $f = 0.1 \text{ MHz}$)	C_{ob}	–	2000 1200	pF
Small–Signal Current Gain ($I_C = 10 \text{ Adc}$, $V_{CE} = 5.0 \text{ Vdc}$, $f = 1.0 \text{ kHz}$)	h_{fe}	15	–	

*Indicates JEDEC Registered Data.

Note 2: Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2.0\%$.



FOR CURVES OF FIGURES 3 & 6, R_B & R_L ARE VARIED.
INPUT LEVELS ARE APPROXIMATELY AS SHOWN.
FOR NPN CIRCUITS, REVERSE ALL POLARITIES.

Figure 2. Switching Time Test Circuit

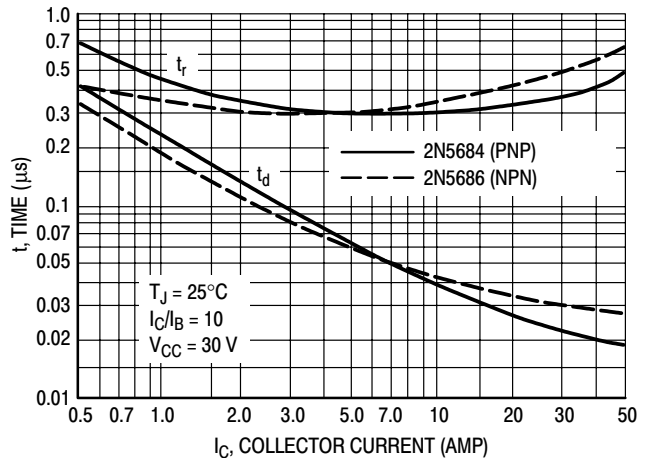


Figure 3. Turn–On Time

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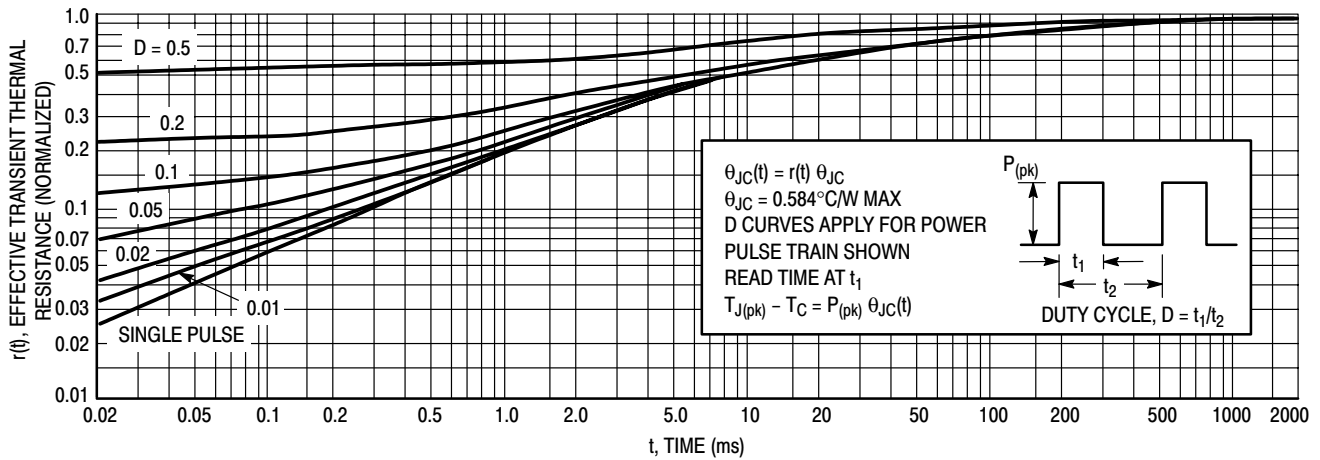


Figure 4. Thermal Response

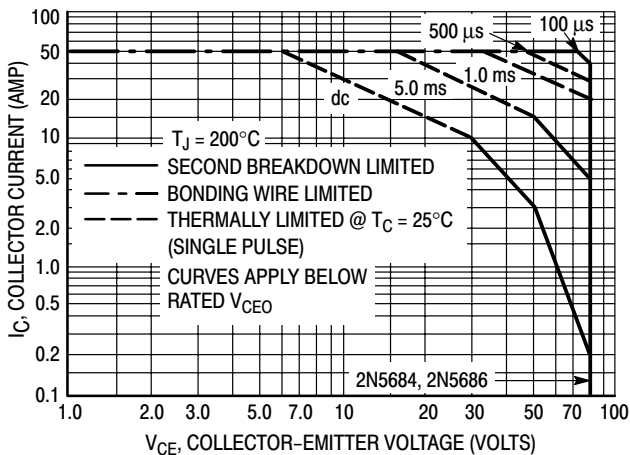


Figure 5. Active-Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^{\circ}\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200^{\circ}\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

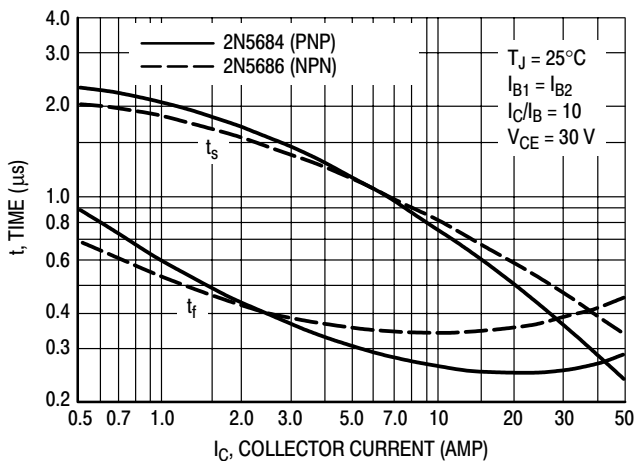


Figure 6. Turn-Off Time

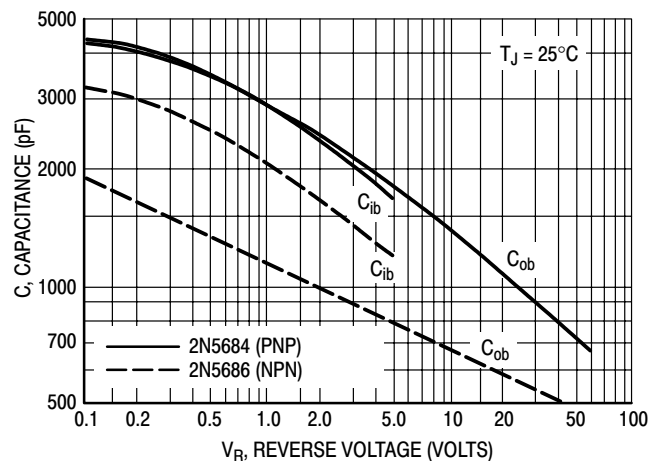
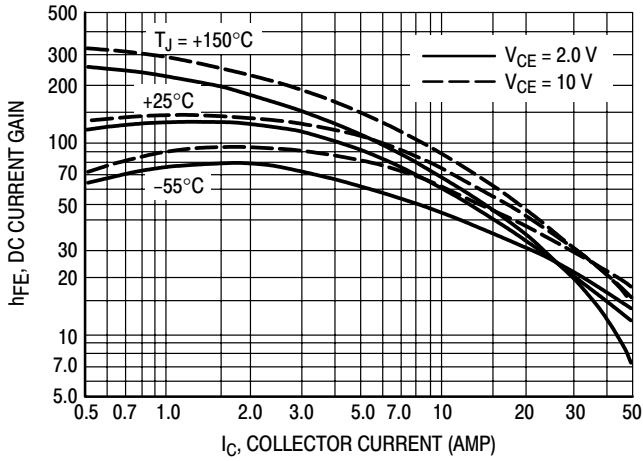


Figure 7. Capacitance

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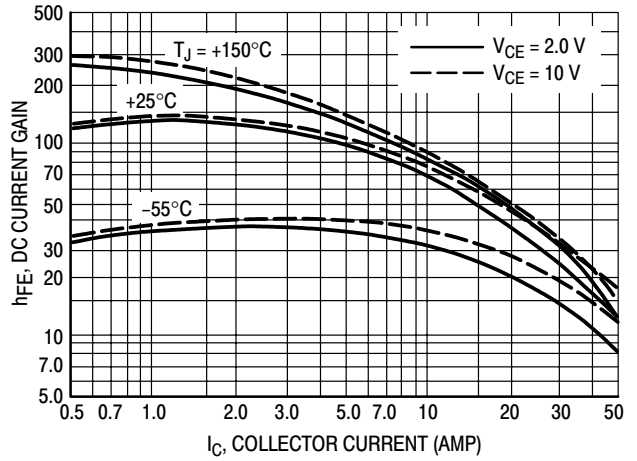


Figure 8. DC Current Gain

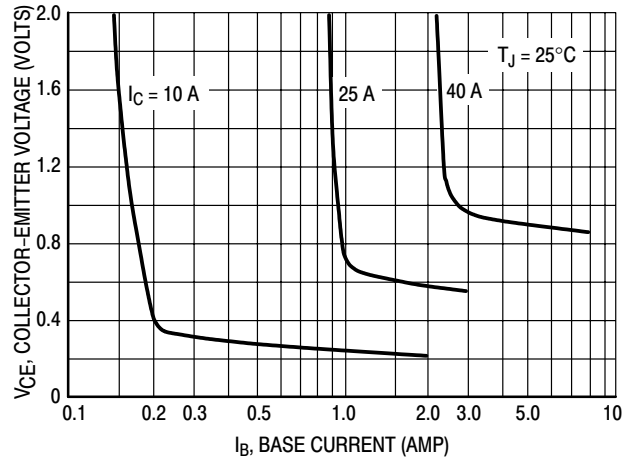
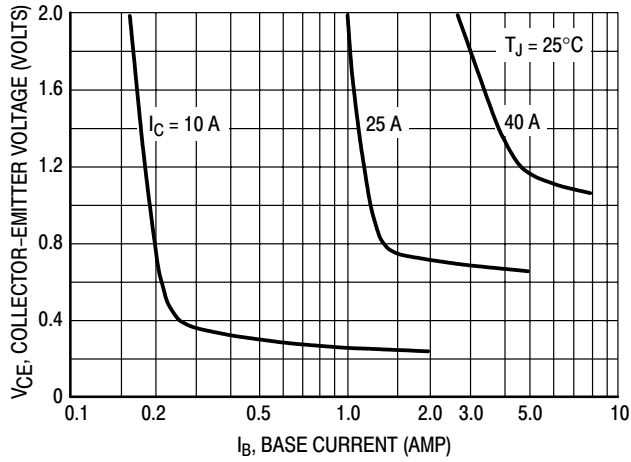


Figure 9. Collector Saturation Region

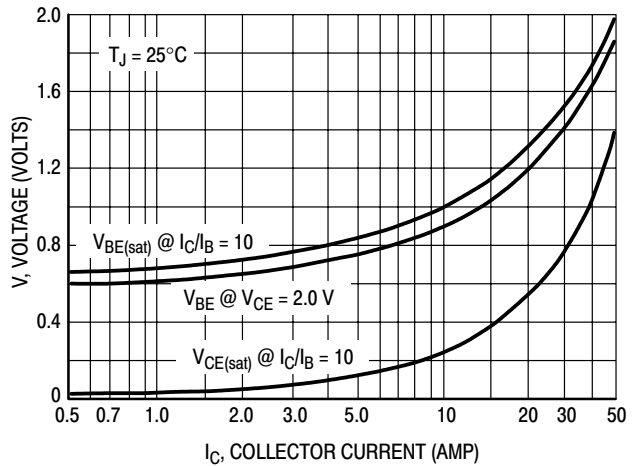
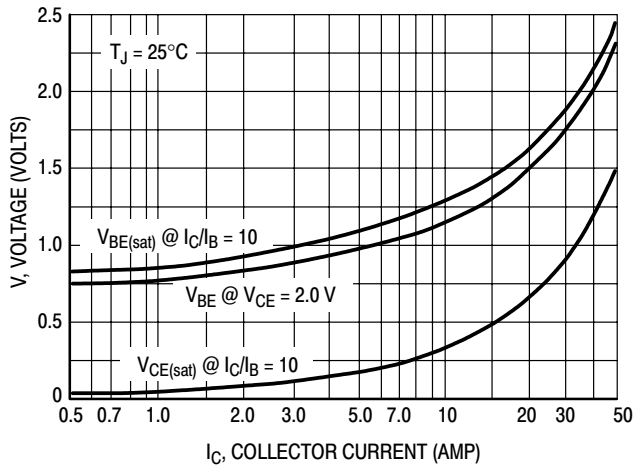
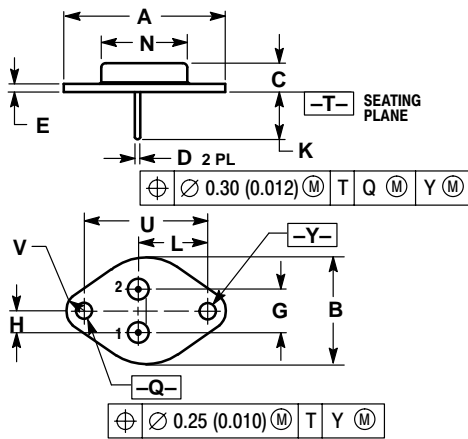


Figure 10. "On" Voltages

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PACKAGE DIMENSIONS

CASE 197A-05
TO-204AE
ISSUE J




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.530 REF		38.86 REF	
B	0.990	1.050	25.15	26.67
C	0.250	0.335	6.35	8.51
D	0.057	0.063	1.45	1.60
E	0.060	0.070	1.53	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	0.760	0.830	19.31	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

Notes

Notes

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